CLAIMS

Please amend claims 1, 8, 21, 25, 39 and 43, and cancel claims 2, 3, 6, 7, 22, 23, 24, 40, 41 and 42 without prejudice or disclaimer:

1. (currently amended) A system for use in a mobile communications device, said system comprising:

a microprocessor having components for responding to interrupt requests by interrupting current processing and performing an interrupt service routine associated with the interrupt request;

peripheral processing units having components for generating interrupt requests for sending to the microprocessor; and

an interrupt controller having components for receiving interrupt requests directed to the microprocessor from the peripheral processing units and for prioritizing the interrupt requests on behalf of the microprocessor,

wherein said interrupt controller includes:

an interrupt source interface unit for receiving interrupt requests directed to the microprocessor from the peripheral processing units;

an interrupt prioritization unit for identifying an interrupt request of highest priority from among the interrupt requests received; and

a microprocessor notification unit for notifying the microprocessor of the interrupt request of highest priority,

wherein said microprocessor notification unit includes:

an interrupt staging unit for storing a value representative of the interrupt request of highest priority; and

an interrupt transmission unit for transmitting a notification signal to the microprocessor indicating that a new interrupt request is stored in the interrupt storage means, and

wherein the microprocessor includes:

an interrupt notification signal reception unit;

interrupt access unit for reading the value representative of the new interrupt request stored within the interrupt staging unit;

a context storage unit for saving a current context of the microprocessor;

an interrupt stack controller for determining whether a current interrupt service routine is being executed, and, if so, for storing the interrupt request associated therewith in an interrupt stack; and

an interrupt service routine execution unit for executing an interrupt service routine associated with the new interrupt request value read from the interrupt staging unit, wherein the interrupt service routine execution unit also detects completion of the interrupt service routine, determines whether the interrupt staging unit contains another value representative of an interrupt request and, if so, executes an interrupt service routine associated with the interrupt request value read from the interrupt staging unit and, if not, retrieves an interrupt request, if any, stored at the top of the interrupt stack and the context saved in the context storage unit and resumes execution based upon that context.

2. (cancel)

3. (cancel)

4. (original) The system of claim 3, wherein the interrupt staging unit is an interrupt vector register.

5. (original) The system of claim 3, wherein the notification signal is an IRQ signal.

6. (cancel)

7. (cancel)

8. (currently amended) The system of claim [7] 1, wherein the interrupt controller also includes:

an interrupt service routine tracking unit for tracking the priority level associated with the interrupt request, if any, currently being processed by the microprocessor;

an interrupt stack tracking unit for tracking the priority level associated with the interrupt request, if any, stored at the top of the interrupt stack of the microprocessor; and

a control unit for:

controlling said interrupt notification unit to store the value representative of the interrupt request of highest priority received by the interrupt controller in the interrupt staging unit only if the priority level associated therewith is higher than the priority level associated with the interrupt request, if any, stored at the top of the interrupt stack of the microprocessor, and

controlling said interrupt transmission unit to transmit the notification signal only if the priority associated therewith is higher than the priority level associated with the interrupt request, if any, currently being processed by the microprocessor.

9. (original) The system of claim 8, wherein said interrupt service routine tracking unit additionally tracks the priority levels of other interrupt requests, if any, stored within the interrupt stack of the microprocessor.

10. (original) The system of claim 9, wherein the interrupt service routine tracking unit detects whether the interrupt staging unit contains an interrupt request when the interrupt access unit of the microprocessor accesses the interrupt staging unit and, if so, resets the highest priority level tracked in the interrupt service routine tracking unit to the highest priority level currently tracked by the interrupt stack tracking unit and, if not, eliminates the highest priority level tracked in the interrupt service routine tracking unit.

11. (original) The system of claim 8, wherein said interrupt service routine tracking unit additionally tracks the priority levels associated with interrupt requests, if any, previously retrieved by the microprocessor but not yet fully processed.

12. (original) The system of claim 11, wherein the interrupt service routine tracking unit detects whether the interrupt staging unit contains an interrupt request when the interrupt access unit accesses the interrupt staging unit and, if so, resets the highest priority level tracked in the interrupt service routine tracking unit to the priority level of the interrupt request

stored in the interrupt request storage unit and, if not, eliminates the highest priority level tracked in the interrupt service routine tracking unit.

13. (original) The system of claim 9, wherein said interrupt stack tracking unit includes an IN_STACK register having at least one bit for each priority level.

14. (original) The system of claim 11, wherein said interrupt service routine tracking means includes an IN_SERVICE register having at least one bit for each priority level.

15. (original) The system of claim 1, wherein said interrupt prioritization unit determines a relative priority of interrupt requests from among a plurality of priority levels.

16. (original) The system of claim 15, wherein said interrupt source interface unit is connected to a plurality of individual interrupt lines, each carrying a separate interrupt request, and

wherein said interrupt prioritization unit includes prioritization registers maintaining a predetermined priority level associated with each of said individual interrupt lines and a plurality of interrupt level slice units associating the predetermined priority level with the received interrupt request based upon the interrupt request line upon which the interrupt is received.

17. (original) The system of claim 16, wherein a plurality of said interrupt level slice units are provided, one per respective priority level, each receiving a value

representative of all interrupt requests and outputting a value representative of only those interrupt requests having the respective priority level.

18. (original) The system of claim 16, wherein said interrupt prioritization unit includes round-robin selection unit for selecting one interrupt among a group of interrupts of each priority.

19. (original) The system of claim 1, wherein the microprocessor includes a power control unit and wherein the interrupt controller additionally includes a power up initiation unit for identifying received interrupt requests authorized to trigger powering up of the microprocessor and for triggering the power control unit to power up the microprocessor in response to receipt of one of said requests.

20. (original) The system of claim 1, wherein said interrupt prioritization unit distinguishes between IRQ and FIQ requests and wherein interrupt notification unit notifies the microprocessor of FIQ requests immediately and independently of IRQ requests.

21. (currently amended) A system for use in a mobile communications device, said system comprising:

a microprocessor having components for responding to interrupt requests by interrupting current processing and performing an interrupt service routine associated with the interrupt request;

peripheral processing units having components for generating interrupt requests for sending to the microprocessor; and

an interrupt controller having:

means for receiving interrupt requests directed to the microprocessor, said interrupt request requesting the microprocessor to interrupt current processing and perform an interrupt service routine associated with the interrupt request;

means for identifying an interrupt request of highest priority from among the interrupt requests received; and

means for notifying the microprocessor of the interrupt request of highest priority,

wherein said means for notifying the microprocessor includes:

interrupt storage means for storing a value representative of the interrupt request of highest priority; and

means for transmitting a notification signal to the microprocessor indicating that a new interrupt request is stored in the interrupt storage means,

wherein the microprocessor includes:

means for receiving the notification signal;

interrupt access means for reading the value representative of the new interrupt request stored within the interrupt storage means;

means for saving a current context of the microprocessor;

means for determining whether a current interrupt service routine is being executed and, if so, for storing the interrupt request associated therewith in an interrupt stack;

means for executing an interrupt service routine associated with the new interrupt request value read form the interrupt storage means;

means for detecting completion of the interrupt service routine; and

means for determining whether the interrupt storage means of the interrupt controller contains another value representative of an interrupt request and, if so, for executing an interrupt service routine associated with the interrupt request value read from the interrupt storage means and, if not, for retrieving an interrupt request, if any, stored at the top of the interrupt stack and the context saved in the means for saving a current context and for resuming execution based upon that context.

22. (cancel)

23. (cancel)

24. (cancel)

25. (currently amended) The system of claim [24] 21, wherein the interrupt controller further includes:

interrupt service routine tracking means for tracking the priority level associated with the interrupt request, if any, currently being processed by the microprocessor;

interrupt stack tracking means for tracking the priority level associated with the interrupt request, if any, stored at the top of the interrupt stack of the microprocessor;

means for controlling said means for notifying the microprocessor to store the value representative of the interrupt request of highest priority received by the interrupt controller in the interrupt storage means only if the priority level associated therewith is higher than the priority level associated with the interrupt request, if any, stored at the top of the interrupt stack of the microprocessor; and

means for controlling said means for transmitting a notification signal to the microprocessor to transmit the notification signal only if the priority associated therewith is higher than the priority level associated with the interrupt request, if any, currently being processed by the microprocessor.

26. (original) The system of claim 25, wherein said interrupt service routine tracking means additionally tracks the priority levels of other interrupt requests, if any, stored within the interrupt stack of the microprocessor.

27. (original) The system of claim 26, wherein the interrupt service routine tracking means includes means for detecting whether the interrupt storage means contains an interrupt request when the interrupt access means accesses the interrupt storage means and, if so, for resetting the highest priority level tracked in the interrupt service routine tracking means to the highest priority level currently tracked by the interrupt stack tracking means and, if not, for eliminating the highest priority level tracked in the interrupt service routine tracking means.

28. (original) The system of claim 25, wherein said interrupt service routine tracking means additionally tracks the priority levels associated with interrupt request, if any, previously retrieved by the microprocessor but not yet fully processed.

29. (original) The system of claim 28, wherein the interrupt service routine tracking means includes means for detecting whether the interrupt storage means contains an interrupt request when the interrupt access means accesses the interrupt storage means and, if so, for resetting the highest priority level tracked in the interrupt service routine tracking means to the priority level of the interrupt request stored in the interrupt request storage means and, if not, for eliminating the highest priority level tracked in the interrupt service routine tracking means.

30. (original) The system of claim 26, wherein said interrupt stack tracking means includes a register having at least one bit for each priority level.

31. (original) The system of claim 28, wherein said interrupt service routine tracking means includes a register having at least one bit for each priority level.

32. (original) The system of claim 21, wherein said means for identifying an interrupt request of highest priority from among the interrupt requests received includes means for determining a relative priority of interrupt requests from among a plurality of priority levels.

33. (original) The system of claim 32, wherein said means for receiving interrupt requests directed to the microprocessor is connected to a plurality of individual interrupt lines, each carrying a separate interrupt request, and

wherein said means for determining the priority relative priority of interrupt requests from among a plurality of priority levels includes means for maintaining a predetermined priority level associated with each of said individual interrupt lines and means for

associating the predetermined priority level with the received interrupt request based upon the interrupt request line upon which the interrupt is received.

34. (original) The system of claim 33, wherein said means for associating the predetermined priority level with the received interrupt request based upon the interrupt request line upon which the interrupt is received includes a plurality of interrupt level slice means, one per respective priority level, each for receiving a value representative of all interrupt requests and outputting a value representative of only those interrupt requests having the respective priority level.

35. (original) The system of claim 33, wherein said means for identifying an interrupt request of highest priority from among the interrupt requests includes means for selecting on interrupts from among a group of interrupts of equal priority.

36. (original) The system of claim 35, wherein the means for selecting one of the interrupts of equal priority is a round-robin selection unit.

37. (original) The system of claim 21, wherein the microprocessor includes means for entering a power shut down mode and wherein the interrupt controller additionally includes means for identifying received interrupt request authorized to trigger powering up of the microprocessor and means for powering up the microprocessor in response to receipt of one of said requests.

38. (original) The system of claim 21, wherein said means for identifying an interrupt request of highest priority from among the interrupt requests received includes means for distinguishing between IRQ and FIQ requests, and

wherein said means for notifying the microprocessor of the interrupt request of highest priority notifies the microprocessor of FIQ requests immediately and independently of IRQ requests.

39. (currently amended) A method for use with an interrupt controller and a microprocessor within a mobile communications device, said microprocessor including components for responding to interrupt requests by interrupting current processing and performing an interrupt service routine associated with the interrupt request, said method comprising the steps of:

receiving interrupt requests directed to the microprocessor using the interrupt controller;

identifying an interrupt request of highest priority from among the interrupt requests received, using the interrupt controller; [and]

notifying the microprocessor of the interrupt request of highest priority;

storing a value representative of the interrupt request of highest priority in an interrupt storage device;

transmitting a notification signal to the microprocessor indicating that a new interrupt request is stored in the interrupt storage means;

receiving the notification signal;

reading the value representative of the new interrupt request stored within the interrupt storage device;

saving a current context of the microprocessor;

determining whether a current interrupt service routine is being executed and, if so, storing the interrupt request associated therewith in an interrupt stack;

executing an interrupt service routine associated with the new interrupt request value read from the interrupt storage device;

detecting completion of the interrupt service routine; and

determining whether the interrupt storage device of the interrupt controller contains another value representative of an interrupt request and, if so, executing an interrupt service routine associated with the interrupt request value read from the interrupt storage device and, if not, retrieving an interrupt request, if any, stored at the top of the interrupt stack and the context associated therewith and resuming execution based upon that context.

40. (cancel)

41. (cancel)

42. (cancel)

43. (currently amended) The method of claim [42] 39, further including the steps performed by the interrupt controller of:

tracking the priority level associated with the interrupt request, if any, currently being processed by the microprocessor within an interrupt service routine tracking device;

tracking the priority level associated with the interrupt request, if any, stored at the top of the interrupt stack of the microprocessor with an interrupt stack tracking device;

storing the value representative of the interrupt request of highest priority received by the interrupt controller in the interrupt storage device only if the priority level associated therewith is higher than the priority level associated with the interrupt request, if any, stored at the top of the interrupt stack of the microprocessor; and

transmitting the notification signal to the microprocessor only if the priority associated therewith is higher than the priority level associated with the interrupt request, if any, currently being processed by the microprocessor.

44. (original) The method of claim 43, wherein further including the step of tracking the priority levels of other interrupt requests, if any, stored within the interrupt stack of the microprocessor.

45. (original) The method of claim 44, wherein the stop tracking interrupt service routines includes the steps of detecting whether the interrupt storage device contains an interrupt request when accessed by the microprocessor and, if so, resetting the highest priority level tracked in the interrupt service routine tracking device to the highest priority level currently tracked by the interrupt stack tracking device and, if not, for eliminating the highest priority level tracked in the interrupt service routine tracking device.

46. (original) The method of claim 43, further including the step of tracking the priority levels associated with interrupt requests, if any, previously retrieved by the microprocessor but not yet fully processed.

47. (original) The method of claim 46, wherein the step of tracking interrupt requests currently being processed by the microprocessor includes the step of detecting whether the interrupt storage device contains an interrupt request when the interrupt access device is accessed by the microprocessor and, if so, resetting the highest priority level tracked in the interrupt service routine tracking device to the priority level of the interrupt request stored in the interrupt request storage device and, if not, eliminating the highest priority level tracked in the interrupt service routine tracking device.

48. (original) The method of claim 39, wherein said step of identifying an interrupt request of highest priority from among the interrupt requests received includes the step of determining a relative priority of interrupt requests from among a plurality of priority levels.

49. (original) The method of claim 48, wherein said step of receiving interrupt requests directed to the microprocessor includes the step of receiving signal simultaneously from a plurality of individual interrupt lines, each carrying a separate interrupt request, and

wherein said step of determining the priority relative priority of interrupt requests from among a plurality of priority levels includes the steps of maintaining a predetermined priority level associated with each of said individual interrupt lines and associating the

predetermined priority level with the received interrupt request based upon the interrupt request line upon which the interrupt is received.

50. (original) The method of claim 49, wherein said step of associating the predetermined priority level with the received interrupt request based upon the interrupt request line upon which the interrupt is received includes the step of routing the signals through a plurality of interrupt level slice units, one per respective priority level, each for receiving a value representative of all interrupt requests and outputting a value representative of only those interrupt requests having the respective priority level.

51. (original) The method of claim 49, wherein if there are more than one pending interrupt requests of equal priority, said step of identifying an interrupt request of highest priority from among the interrupt requests includes the step of selecting one of the interrupts of equal priority via a round-robin selection process.

52. (original) The method of claim 39, wherein the microprocessor additionally performs the step of entering a power shut down mode and wherein the interrupt controller additionally performs the step of identifying received interrupt requests authorized to trigger powering up of the microprocessor and powering up the microprocessor in response to receipt of one of said requests.

53. (original) The method of claim 39, wherein step of identifying an interrupt request of highest priority from among the interrupt requests received includes the step of distinguishing between IRQ and FIQ requests and wherein said step of notifying the

microprocessor of the interrupt request of highest priority is performed to notify the microprocessor of FIQ requests immediately and independently of IRQ requests.